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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/002,265	12/31/97	VAN DER WAL G	DSRC-0005/SA

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EXAMINER	
BROWN, R	
ART UNIT	**PAPER NUMBER**
2711	13

DATE MAILED: 02/16/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/002,265	Van Der Wal
Examiner	**Group Art Unit**
Reuben M. Brown	2711

☒ Responsive to communication(s) filed on *Dec 7, 1999* .

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-30* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1, 12-25, and 27-30* is/are rejected.

☒ Claim(s) *2-11 and 26* is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☒ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 20-22, 24-25, 27-28 & 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove (U.S. Pat # 5,768,609)., in view of Katsura (U.S. Pat # 5,046,023).

Considering claim 1, Gove discloses all subject matter including at least processing module containing at least one general purpose microprocessor, as a plurality of image processing systems, i.e. ISP nodes 30-32 are disclosed, wherein each image processing system comprises a master processor 12, which controls hardware and software operation of the video processing system using control data, and which also processes video data, (Fig. 1; Fig. 3; col. 8, lines 51-65; col. 13, lines 20-60; col. 14, lines 56-68; col. 16, lines 3-7). The claimed video processing module which contains parallel pipelined video hardware components, wherein the video processing

module is responsive to the control data to perform different video processing operations on the video data is met by the parallel processors 100-10n, (col. 9, lines 47-57; col. 13, lines 51-67; col. 14, lines 1-55; col. 16, lines 7-21). The amended claimed global video bus which establishes a direct connection between the processing module and at least one video processing module to route the video data between the processing module and the at least one video processing module is met by the crossbar switch 20, which provides the parallel processors with video data memory 10. Regarding the claimed global control bus which is separate from the global video bus, and which provides configuration data to/from the processing module to the at least one video processing module is met by Gove, (col. 2, lines 52-64; col. 6, lines 11-39; col. 7, lines 25-65; co. 36, lines 4-27; col. 38, lines 34-64), even though Gove teaches that the communication bus 40 transmits synchronization signals to the parallel processors, the reference does not explicitly state whether configuration data may also be transmitted on the instant bus. Nevertheless, at the time the invention was made, the technique of transmitting data on one bus and control/configuration data on a separate bus was notoriously well known in the art and is in fact well known standard practice in the art of data transmission internal to a computer/multiprocessor system. Katsura provides an illustration of such a technique, (Fig. 1; col. 8, lines 21-25, lines 42-52). Katsura shows that a system bus may be drawn displaying data and control either separate or combined, with either design being obvious over the other. Therefore it would have been obvious for one of ordinary skill in the art at the time the invention was made to modify Gove, with the teachings of

Katsura showing data bus and control/configuration bus as being separate, at least for the well known benefit of advantages of utilizing a so-called 'dedicated bus'.

Considering claim 20, the claimed method steps of creating a modular video processing system which corresponds with subject matter cited above in the rejection of claim 1, are likewise rejected. Regarding the additional claimed limitation of the parallel pipelined hardware being responsive to configuration data reads on Gove, (col. 13, lines 20-35). The further claimed limitation of the processing module detecting the presence of each video processing module connected to the global configuration bus, and passing the configuration data to each detected video processing module over the global configuration bus also inherently included in Gove, (col. 9, lines 35-31; col. 13, lines 20-35).

Considering claims 21 & 28, the claimed feature of crosspoint switch is met by the individual parallel processors' connection to the crossbar 20, (Fig. 1; Fig. 4; col. 6, lines 47-52; col. 7, lines 25-44). Gove does not specifically discuss a system clock, however such a feature which provides timing signals associated with video data is inherently included in Gove, which discloses that data is cycled through the various processors, in a synchronous or asynchronous manner (col. 3, lines 4-14; col. 6, lines 11-20; col. 12, lines 16-29). The claimed feature of timing signals which indicate that video data is active at least reads on the sync signal, which informs the processors that it is OK to execute code with respect attendant video data, (col. 21, lines 35-51).

Considering claim 22, the claimed synchronous start signal reads on Gove, (col. 20, lines 1-12; col. 21, lines 36-50).

Considering claim 24, the claimed state machine which monitors the transfer of video data and facilitates the allocation of paths for transferring among parallel processors, reads on the state machine 5708, included within the transfer processor 11, which monitors the block transfer of video data in the ISP nodes, (Fig. 57; col. 57, lines 61-67 thru col. 58, lines 1-21), in conjunction with the crossbar memories 10 and crossbar switch matrix 20.

Considering claims 25 & 30, the claimed configuration data which comprises respective control signals for each hardware component of the video or specialized processing system, such that each processing module manipulates the control signals to program the instant hardware components for each of the different specialized video processing operations corresponds to subject matter recited above in the rejection of claim 19, with respect to the hardware control library, and is likewise rejected.

Considering claim 27, the claimed features which correspond with subject matter recited above in the rejection of claims 1 & 20, are likewise rejected. Regarding the differences, the claimed at least one specialized processing module which contains parallel pipelined hardware that is programmable to provide different specialized processing operations on an input stream, reads

on any particular ISP node, which contains a plurality of DSP processors which may currently perform different video processing operations on video data. The claimed general purpose microprocessor which has a hardware control library loaded thereon, wherein the hardware control library comprises a set of functions for programming the parallel pipelined hardware of the at least one specialized processing module such that the microprocessor performs predetermined specialized processing operations on the input data, reads on the operation of master processor 12, which comprises at least a register file 2901, opcode instructions 2911 and control logic 2904, which controls the microprocessor according to the instruction loaded. These instant loaded instructions enable the master processor 12 to schedule and control all video processing operations by the DSP parallel processors, (Fig. 29; col. 13, lines 20-37; col. 34, lines 53-64).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12-19, 23 & 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove & Katsura, in view of Trimberger, (U.S. Pat # 5,652,904).

Considering claim 12, Gove discloses in Fig. 3, a modular video processing system which may comprise a plurality of image processing systems, or ISP chip nodes, wherein the ISP chip nodes contain the circuits as shown in Fig. 1 & Fig. 2, which include a microprocessor as master processor 12, (col. 3, lines 39-44; col. 8, lines 51-66). One of ordinary skill in the art at the time the invention was made, would have readily recognized the benefit of utilizing a plurality of microprocessors in a particular system, in order to increase the productivity of the system, since different microprocessors would be enabled to at least operate on different instructions simultaneously. Recognizing such a benefit, Gove discloses at least one embodiment, in which in addition to the master processor 12, one of the plurality of parallel processors 100-103, will act as the "master" processor and perform instruction fetches on behalf of all the other PP's, (col. 35, lines 58-67; col. 36, lines 47-67). However, even though Gove does not specifically disclose using more than one *microprocessor* in an ISP node, the technique of utilizing at least two microprocessors in one particular processing system, at least in a manner in which functions are shared or divided between the two instant microprocessors, which increases the speed and calculating capability of the instant system, was notoriously well known in the art at the time the invention was made, and is taught by Trimberger, (Fig. 5; col. 1, lines 60-67; col. 3, lines 12-21; col. 10, lines 16-46). Therefore it would have been obvious to one of ordinary skill in the art at

the time the invention was made to modify Gove & Katsura, to include at least two microprocessors within a single processing system, as taught by Trimberger, for the known benefit of improving the performance of a microcontrolled system. The claimed step of coordinating multitask operations of the two microprocessors is necessarily included in the combination of Gove and Trimberger. Gove discloses that the plurality of ISP nodes may access a single global memory, (col. 8, lines 59-64). The claimed arbiter control bus is met by the bus 34, of Gove. Furthermore, Trimberger discloses that each microprocessor within a multiprocessor system, may be enabled to maintain a portion of its memory that is unshared by the other microprocessors in the instant multiprocessor system, (col. 12, lines 6-13).

Considering claim 13, Gove discloses that the plurality of parallel processors may provide various video processing functions are begin execution based on the sync signal, (col. 9, lines 47-57; col. 20, lines 1-11; col. 21, lines 37-50; col. 42, lines 12-24; col. 60, lines 41-47).

Considering claim 14, Gove discloses that the video processors may receives input/output at least from a camera and display, which reads on a communication interface with external devices. The claimed arbiter control bus which controls access to the external devices from the plurality of processors is necessarily included in Gove.

Considering claim 15, Gove discloses that memory 10, associated with a particular microprocessor is connected to a global video bus, (col. 7, lines 16-22).

Considering claim 16, Gove introduces a system in which a plurality of microprocessors might be utilized to improve the performance of a modular video processing system. As noted above in the rejection of claim 12, the combination of Gove and Trimberger provides a processing system with at least two microprocessors operating in conjunction, for the known advantages of a more efficient system. The claimed additional feature of a semaphore register, which at least facilitates the coordination of mutually exclusive operations by the instant at least two microprocessors, reads on the semaphores utilized by Gove, disclosed at least in the MIMD mode, (col. 41, lines 51-57).

Considering claim 17, regarding the claimed feature of a hardware control library which comprises functions for programming the parallel pipelined hardware to function concurrently, Gove teaches that the master processor 12 has access to all memory and operates the scheduling and control of the entire system or node, (col. 13, lines 30-38; Fig. 29). Gove discloses that the different video processing procedures operate concurrently, (col. 9, lines 47-57; col. 20, lines 1-11; col. 35, lines 31-57).

Considering claim 18, Gove teaches that the plurality of ISP nodes, each of which may contain a microprocessor, operate concurrently, (col. 8, lines 63-67).

Considering claim 19, the claimed control signals which controls each hardware component, is inherent in Gove, (col. 8, lines 13-37).

Considering claim 23, the claimed method steps corresponds with subject matter rejected above in claim 16, and is likewise rejected.

Considering claim 29, the claimed feature of a processing module comprising at least two general purpose microprocessors corresponds with subject matter mentioned above in the rejection of claim 12, and is likewise rejected. Trimberger teaches that multiple microprocessors may be added to a system in which the speed of a single microprocessor would not be sufficient to handle many instructions at a sufficient clock speed, which reads on the claimed limitation of concurrent multitask processing operations of at least two microprocessors, (col. 10, lines 16-20).

Allowable Subject Matter

5. Claims 2-11 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments with respect to claims 1, 20, 21, 24, 27 & 28 have been considered but are moot in view of the new ground(s) of rejection.

Regarding applicant's arguments with respect to claims 1, 20 & 27, examiner points out the applicants claim language recites; "a modular video system comprising" & "method of creating a modular video processing system, comprising the steps of:" Thus, the system of claims 1, 20 & 27, does not limit the elements/functions of the global video bus to only establishing " a direct connection between the processing module and at least one video processing module to route the video data between said processing module and said at least one video processing module". Applicant argues on page 6 & page 7, that Grove discloses that configuration data, i.e

program instructions are accessed by the parallel processors via the crossbar switch, as well as image and graphic data over the instant crossbar switch, which means that the global control bus is not separate from the global video bus, examiner respectfully disagrees, since Grove provides at least one global control bus, i.e synchronization bus 40, which is separate from the global video bus, i.e crossbar switch 20.

Moreover, Grove specifically states that the master processor 12 is connected to data cache 13 and instruction cache 14, which reads on the claimed hardware control library, (col. 6, lines 31-36). Examiner respectfully disagrees with applicant's assertion on page 6, 4th paragraph and page 7, 1st paragraph that Grove does not disclose or suggest transmitting any synchronization data or any control data from a hardware control library via the communication bus 40. The claimed limitation: "a global control bus which provides data to/from said hardware control library of said general processing module from/to said at least one specialized processing module separate from said stream input data" is met by Grove, since the master processor 12 transmits instructions to the parallel processors via the communication channel or bus 40, (col. 13, lines 20-38).

Regarding applicant's argument with respect to claims 21 & 28. On page 8, 1st paragraph, applicant argues that the sync signals are only provided to the parallel processors via the communication bus 40 and is thus separate from the video data signal. However, examiner agrees

with applicant's earlier assertion on page 6, 4th paragraph that "the contents of the synchronization registers and the registers which hold addresses of the other processors to which the one processor is synchronized are set from program instructions that are fetched by the processor via the crossbar switch 20". Furthermore examiner contends that video data, which applicant does not dispute is transmitted via the crossbar switch 20, inherently includes timing and synchronization signals such as but not limited to: horizontal and vertical synchronization signals & horizontal and vertical blanking interval pulses.

In response to applicant's argument with respect to claim 24 on page 7, 5th paragraph that the references fail to show certain features of applicant's invention, it is noted that the feature upon which applicant relies (i.e., applicant mentions a crosspoint switch internal to each parallel processor). This limitation is not recited in the rejected claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

7. Applicant's arguments with respect to the Muramatsu reference have been considered but are moot in view of the new ground(s) of rejection.

8. Applicant's arguments filed 12/7/99, with respect to the reliance upon the Gove reference, in the rejection of claim 12 have been fully considered but they are not persuasive. On page 10, 4th paragraph applicant argues that Gove does not disclose or suggest "that each microprocessor has an associated RAM which is not shared with any other microprocessor", examiner points out that Trimberger provides such a feature, (col. 12, lines 6-13). Applicant further argues that "even if Gove had two microprocessors, both microprocessors would be connected to the crossbar switch allowing both microprocessors to access all the memories". Examiner respectfully disagrees with the conclusion drawn by the applicant in this instance. In particular, while Trimberger certainly provides an embodiment in which microprocessors in a multiprocessor system are enabled to share memory, Trimberg goes on to suggest that at least for the benefit of efficiency, it would have been desirable for *individual microprocessors to also reserve* a portion of its memory that is unshared with the other microprocessors. Thus even though operating Trimberg within the system of Gove would indeed provide that microprocessors are enabled to access shared memory, for the known advantages of such a technique (whether or not the instant memory is accessed via the crossbar switch as asserted by the applicant), the instant feature does not preclude the further embodiment of Trimberg which provides for *each microprocessor to also* maintain a cache of unshared memory.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's claims.

A) Faroudja, Karlock Provides standard teaching on various synchronization and timing signals inherent in video data.

B) Lockwood Provides teachings on multiprocessor systems and semaphore registers.

C) Thurber, et al Paper which discloses several of the variety of implementations of a data bus, control bus or address bus, including the utilization of so-called 'dedicated buses'.

D) Date High speed parallel processing.

Any response to this action should be mailed to:

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or faxed to:

(703) 308-9051, (for formal communications intended for entry)

Or:

(703) 308-5399 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reuben M. Brown whose telephone number is (703) 305-2399. The examiner can normally be reached on Monday thru Friday from 830am to 430pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Faile, can be reached on (703) 305-4380. The fax phone number for this Group is (703) 308-6306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4700.

VICTOR R. KOSTAK
PRIMARY EXAMINER